What is claimed is:

1. A semiconductor memory device, comprising:

a plurality of memory cells;

a current sense amplifier; and

a feedback circuit to adjust a gain of the current sense amplifier depending on relative delays of data stored in different ones of the memory cells to be read on the current sense amplifier.

2. The device of claim 1, in which the feedback circuit

includes a replica of a reference one of the memory cells, and

is adapted to determine the delay of any one of the reference cells relative to an emulated delay of the reference memory cell.

3. The device of claim 2, in which

each of the memory cells is connected to the amplifier through a data IO line pair, and

the reference memory cell is the one with the shortest data IO line pair.

4. The device of claim 2, in which

the feedback circuit outputs a bias voltage determined by the determined delay, and

the current sense amplifier receives the bias voltage and adjust accordingly the gain.

5. The device of claim 4, in which the feedback circuit includes

an input impedance circuit to generate intermediate output voltages in response to the bias voltage, and

a bias amplifier to generate the bias voltage in response to the intermediate output voltages.

6. A semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells;

a plurality of data IO line pairs connected to a plurality of local data IO line pairs of the memory cell array;

a plurality of first current sense amplifying means for controlling a loop gain in response to a control signal, and for amplifying and outputting a current difference of each of the plurality of the data IO line pairs; and

a current sense amplifier input impedance detecting and loop gain control signal generating means for detecting an input impedance of the plurality of the first current sense amplifying means to generate the control signal when a read command is applied.

7. The device of claim 6, in which the current sense amplifier input impedance detecting and loop gain control signal generating means includes:

a current sense amplifier input impedance detecting means for generating a detecting voltage to detect the input impedance of the plurality of the first sense amplifying means when the read command is applied; and

a loop gain control signal generating means for receiving the detecting voltage to generate the control signal to indicate whether the input impedance is negative or positive.

8. The device of claim 6, in which each of the plurality of the first current sense amplifying means includes:

a first current sense amplifier for amplifying a current difference of the data IO line pair to generate an output voltage and an inverted output voltage; and

a first loop gain control means for being connected between the output voltage and the inverted output voltage of the first current sense amplifier, reducing a voltage difference between the output voltage and the inverted output voltage in response to the control signal when the input resistance is negative, and maintaining a voltage between the output voltage and the inverted output voltage "as is" in response to the control signal when the input impedance is positive.

9. The device of claim 8, in which the first loop gain control means includes a first PMOS transistor.

10. The device of claim 6, in which the current sense amplifier input impedance detecting means includes:

a bit line sense amplifier for amplifying data applied in response to the read command;

a data IO gate for transferring data of the bit line sense amplifier to the data line pair in response to the read command;

a current sense amplifier load circuit for applying an electric current to the data line pair in response to the read command; and

a second sense amplifying means for controlling a loop gain in response to the control signal and amplifying a current difference of the data line pair to generate an output voltage and an inverted output voltage,

in which the bit line sense amplifier, the data IO gate and the current sense amplifier load circuit are configured to have a line load capacitance of from, among the plurality of the memory cells, the memory cell nearest to the first current sense amplifying means to the plurality of the first current sense amplifying means.

11. The device of claim 10, in which the second current sense amplifying means includes:

a second current sense amplifier for amplifying a current difference of the data line pair to generate the output voltage and the inverted output voltage;

a second loop gain control means for being connected between the output voltage and the inverted output voltage of the second current sense amplifier, reducing a voltage difference between the output voltage and the inverted output voltage in response to the control signal when the input resistance is negative, and maintaining a voltage between the output voltage and the inverted output voltage "as is" in response to the control signal when the input impedance is positive.

12. The device of claim 11, in which the second loop gain control means includes a second PMOS transistor.

13. The device of claim 11, in which the loop gain control signal generating means receives data of the data line pair of the current sense amplifier input impedance circuit as the detecting voltage, and lowers a level of the control signal down when the input impedance of the current sense amplifier is negative and raises the level of the control signal up when the input impedance is positive.

14. The device of claim 13, in which the loop gain control signal generating means includes:

a bias means for generating a bias voltage when a power voltage is applied;

a differential amplifier for being enabled when the bias voltage is applied, and amplifying a difference of the detecting voltage to generate the output voltage; and

an output driving circuit for generating the control signal in response to the bias voltage and raising a level of the control signal up in response to the output voltage.

15. A semiconductor memory device, comprising:

a plurality of memory cells connected between a plurality of bit line pairs;

a plurality of sense amplifying means for amplifying data between the plurality of the bit line pairs;

a plurality of data IO gates for transferring data between the plurality of the bit line pairs and a plurality of local data IO line pairs;

a plurality of current sense amplifier load means for being connected between the plurality of the local data IO line pairs and the plurality of the data IO line pairs, and applying an electric current to the plurality of the local data IO line pairs and the data IO line pairs when a read command is applied;

a plurality of first current sense amplifying means for controlling a loop gain in response to a control signal, and amplifying and outputting a current difference of each of the plurality of the data IO line pairs;

a current sense amplifying input resistance detecting means for generating a detecting voltage to detect an input impedance of the plurality of the first current sense amplifying means when the read command is applied; and

a loop gain control signal generating means for receiving the detecting voltage to generate the control signal when the input impedance is negative.

16. The device of claim 15, in which each of the first current sense amplifying means includes:

a first current sense amplifier for amplifying a current difference of the data IO line pair to generate an output voltage and an inverted output voltage; and

a first loop gain control means for being connected between the output voltage and the inverted output voltage of the first current sense amplifier, reducing a voltage difference between the output voltage and the inverted output voltage in response to the control signal when the input resistance is negative, and maintaining a voltage between the output voltage

and the inverted output voltage "as is" in response to the control signal when the input impedance is positive.

17. The device of claim 16, in which the first loop gain control means includes a first PMOS transistor.

18. The device of claim 15, in which the current sense amplifier input impedance detecting means includes:

a bit line sense amplifier for amplifying data applied in response to the read command;

a data IO gate for transferring data of the bit line sense amplifier to the data line pair in response to the read command;

a current sense amplifier load circuit for applying an electric current to the data line pair in response to the read command; and

a second sense amplifying means for controlling a loop gain in response to the control signal and amplifying a current difference of the data line pair to generate an output voltage and an inverted output voltage,

in which the bit line sense amplifier, the data IO gate and the current sense amplifier load circuit are configured to have a line load capacitance of from, among the plurality of the memory cells, the memory cell nearest to the first current sense amplifying means to the plurality of the first current sense amplifying means.

19. The device of claim 18, in which the second current sense amplifying means includes:

a second current sense amplifier for amplifying a current difference of the data line pair to generate the output voltage and the inverted output voltage;

a second loop gain control means for being connected between the output voltage and the inverted output voltage of the second current sense amplifier, reducing a voltage difference between the output voltage and the inverted output voltage in response to the control signal when the input resistance is negative, and maintaining a voltage between the output voltage and the inverted output voltage "as is" in response to the control signal when the input impedance is positive.

20. The device of claim 19, in which the second loop gain control means includes a second PMOS transistor.

21. The device of claim 15, in which the loop gain control signal generating means

receives data of the data line pair of the current sense amplifier input impedance circuit as the detecting voltage, and

lowers a level of the control signal down when the input impedance of the current sense amplifier is negative and raises the level of the control signal up when the input impedance is positive.

22. The device of claim 21, in which the loop gain control signal generating means includes:

a bias means for generating a bias voltage when a power voltage is applied;

a differential amplifier for being enabled when the bias voltage is applied, and amplifying a difference of the detecting voltage to generate the output voltage; and

an output driving circuit for generating the control signal in response to the bias voltage and raising a level of the control signal up in response to the output voltage.

23. A data read method of a semiconductor memory device including a plurality of memory cells, the method comprising:

generating a control signal to control a loop gain of a plurality of current sense amplifiers by detecting a variation of an input impedance of the current sense amplifier when a read command is applied and data are read from the memory cell nearest to the plurality of the current sense amplifiers;

controlling the loop gain of the plurality of the current sense amplifiers in response to the control signal; and

amplifying a current different of each of a plurality of data IO line pairs by the plurality of the current sense amplifiers to generate a plurality of output signals.